

FILED

November 19, 2021

CLERK, U.S. DISTRICT COURT
WESTERN DISTRICT OF TEXAS

**IN THE UNITED STATES DISTRICT COURT
FOR THE WESTERN DISTRICT OF TEXAS
WACO DIVISION**

BY: lad
DEPUTY

Xiaohua Huang, *pro se*

Plaintiff

v.

Intel Corporation

Defendant

Civil Action No.: **6:21-cv-01213**

Jury Trial Requested

**PLAINTIFF XIAOHUA HUANG'S COMPLAINT FOR PATENT
INFRINGEMENT AGAINST INTEL CORPORATION**

NATURE OF THE ACTION

1. This is an action for patent infringement arising out of U.S. Patent No. 6,744,653 (hereinafter the "653 Patent") issued on June 1, 2004 to Plaintiff Xiaohua Huang ("Huang" or "Plaintiff") as the inventor. This action is brought to remedy the infringement of '653patent by Defendant Intel Corporation ("Intel" or "Defendant") for infringement of U.S. Patent No. 6744653 (the "653 patent"). Plaintiff Huang mailed letters and sent emails to Defendant Intel since April 1,2021 on how the Intel's products have infringed the "653 patent".

THE PARTIES

2. Plaintiff is an Individual with a place of residence in Los Gatos, California.

3. Defendant Intel is a corporation with a principal place of business at 2200 Mission College Boulevard, Santa Clara, CA 95054 with Telephone Number: 408 765 8080 and website: <http://www.intel.com>. Defendant Intel has its operation office to do business daily and regularly in this district.

JURISDICTION AND VENUE

3. This action arises under the patent laws of the United States, 35 U.S.C. § 101, et seq. This Court has jurisdiction over the subject matter of this action pursuant to 28 U.S.C. §§ 1331 and 1338(a). Venue is proper in this District pursuant to 28 U.S.C. §§1391(b) - (c) and 1400(b) in that Defendant has its operation office to do business daily and regularly in this District.

BACKGROUND FACTUAL ALLEGATION

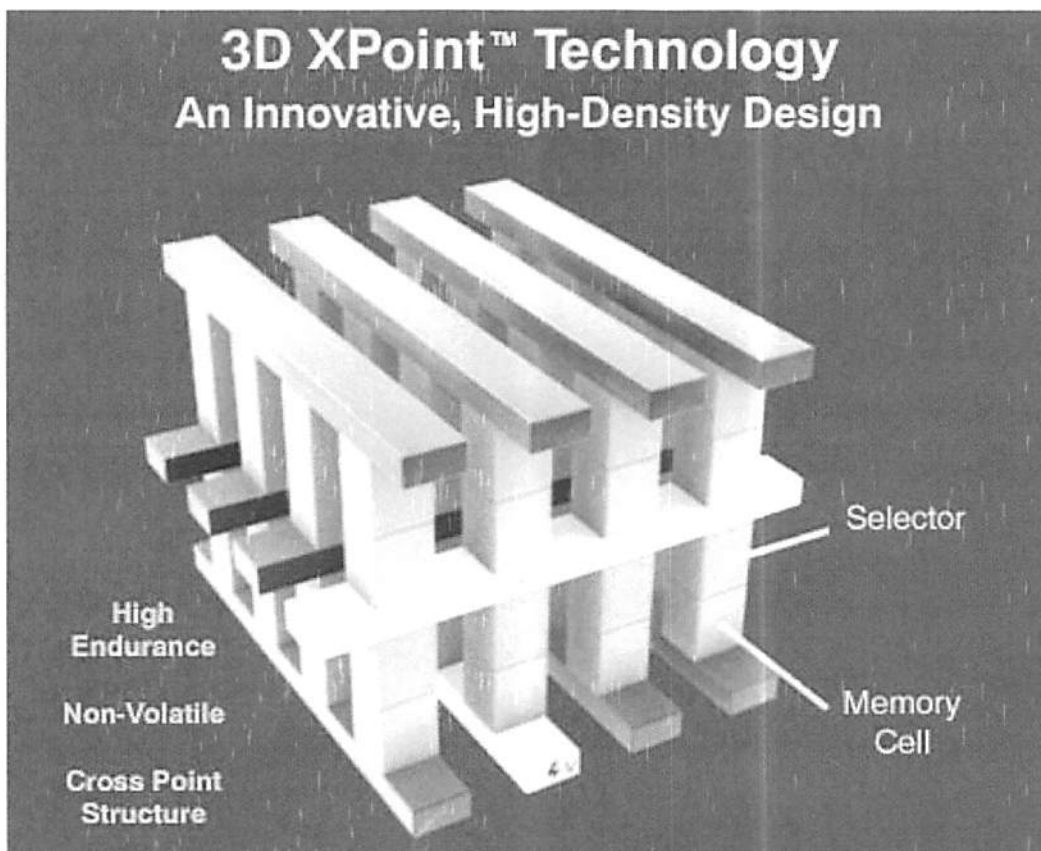
4. A true and correct copy of the '653patent is attached hereto as Exhibit B. The '653patent is valid and owned by Plaintiff Mr. Huang as the inventor.

5. In Nov. 2000 "Huang" found CMOS Micro Device Inc. ("CMOS") to develop Ternary Content Addressable Memory. "Huang" is the owner of "CMOS". From November, 2000 to October, 2002, Huang finished the design of ternary content addressable memory (TCAM) with 0.18um and 90nm TSMC technology which is covered by the '653 Patent. The TCAM designed by Huang is tens to hundreds of times faster in speed and consume much less power than the same products in Market at that time. TCAM invented by Huang has been used by all the networking switches chips now. The circuit and logic claimed in claim 17 of '653patent has been used in Intel Optane product which is also called 3D XPoint memory.

THE INFRINGING PRODUCTS WHICH DEFENDANT MAY HAVE MADE AND SOLD

6. Based on the information obtained that the following picture in Figure1 is the Intel 3D Xpoint resistance memory which Intel branded it as Optane. Intel has made, used and sold Optane memory in NVM chips and Solid State Drive (SSD) two products. In Figure 1 there are two devices in each storage unit, one is "Selector" which is a device when the voltage applied on it is lower than its threshold it does not conduct current, when the voltage applied on it is higher than

its threshold, it conducts current, which function is like a transistor acting as a switch or “Selector”, the other device is a resistance called “Memory Cell”. The resistance value of the “Memory Cell” could be programmed to either “low resistance” called “0” state or “high resistance” called “1” state. When voltage applied to the top and bottom wire of the selector causes the cell to be read or written.



(Image courtesy of Intel) <https://www.pcmag.com/encyclopedia/term/3d-xpoint>

Figure 1. Intel 3D Xpoint Technology (Cross Point Structure)

7. Figure 2 is the reading circuit and logic path of the 3D Xpoint memory, we use the transistor symbol to represent the “Selector” because they both have the function as a switch although made by different material. The metal lines connected to “Selector” are called “Word line” and the white color metal lines connected to “Memory Cell” are called common lines in Figure 2. How to read the information stored in the Resistance “Memory Cell” in Figure 1 is depicted in Figure 2.

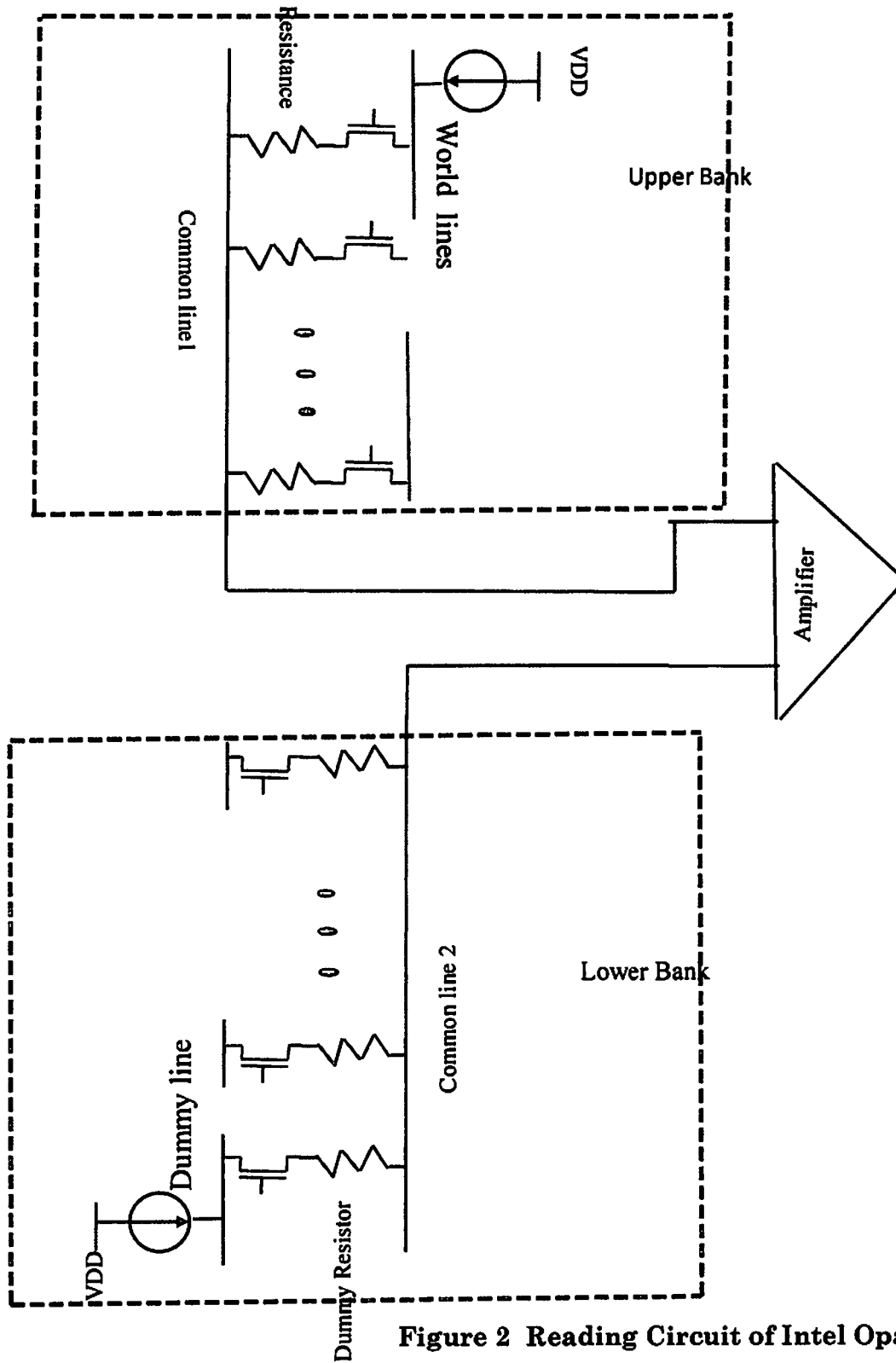


Figure 2 Reading Circuit of Intel Opene Memory

8. In Figure 2 there are same and identical memory array (“Word line” and “common line” in the Upper Bank and the Lower Bank. There are differential read amplifier in the middle, one input of the differential Amplifier connects to the common line in the Upper Bank, the other input of the differential Amplifier connects to the common line in the Lower Bank. When reading the data in the Upper Bank, the common line connecting to Lower Bank act as reference line. When reading the data in the Lower Bank, the common line connecting to Upper Bank act as reference line. In the real memory chips there is a dummy word line connecting to common line through a “Selector” and a “resistor” which has the value which can act as reference in both upper bank and lower band , the dummy world line is enabled and common line in the block (Bank) which is not in read acts as reference line. The circuits in Figure 2 used in “Intel® Optane™ Persistent Memory” are read by the claim 17 of US patent 6744653 under Doctrine of Equivalence. The Claim 17 of US patent 6744653 was about CAM, it also read the circuit in Figure 2 of “Intel® Optane™ Persistent Memory” under Doctrine of Equivalence. The “Word line” here corresponds to the “Match line” in CAM.

HOW CLAIM 17 OF ‘653PATENT READ INTEL® OPTANE™ MEMORY”

9. Claim 17 of ‘653Patent: A method for sensing a logic state of a match line in a content addressable memory (CAM), comprising: sensing a signal on a first common line, wherein the signal on the first common line is related to a signal on the match line; providing a reference signal on a second common line based on a plurality of dummy transistors; determining a difference between the sensed signal on the first common line and the reference signal on the second common line; amplifying the determined difference with a positive feedback amplifier; and providing an output value indicative of the logic state of the match line based on the amplified difference.

(1) *“A method for sensing a logic state of ‘a match line in a content addressable memory (CAM)’, comprising”.*

This is preamble. In reference to Figure 2 where we can make claim section (1) *“A method for sensing a logic state of ‘a match line in a content addressable memory (CAM)’, comprising”.* corresponding to: “A method for sensing a logic state of ‘Memory cell (Resistance) related to the selected word line in Intel Opene Memory’, comprising”. Under Doctrine of equivalence, ‘a match line’ corresponds to ‘Memory cell(Resistance) in the selected word line’ and ‘in a content addressable memory (CAM)’ corresponds to ‘of Intel Opene Memory’.

(2) *sensing a signal on a first common line, wherein the signal on the first common line is related to a signal on the match line;*

In reference to Figure 2 Under Doctrine of Equivalence, ‘the match line’ corresponds to ‘Memory cell(Resistance) related to selected word line’. Under Doctrine of Equivalence this claim section (2) reads common line and the circuits in the Upper Bank in Figure 2.

(3) *providing a reference signal on a second common line based on a plurality of dummy transistors;*

Under Doctrine of Equivalence ‘dummy transistors’ corresponds to “dummy resistances’. Under Doctrine of Equivalence this claim section (3) reads on the circuits of lower bank in Figure 2.

(4) *determining a difference between the sensed signal on the first common line and the reference signal on the second common line;*

This claim section (4) read the two common lines in Figure 2.

(5) *amplifying the determined difference with a positive feedback amplifier;*

This claim section (5) read the amplifier in Figure 2.

(6) *and providing an output value indicative of the logic state of the match line based on the amplified difference.*

Where “the match line” corresponds to “Memory Cell (Resistance) related to selected word line”. This claim section (5) read the circuit in Figure 2 under Doctrine of Equivalence.

10. The circuit in Figure 1 and Figure 2 are embedded inside in the chips of the following Intel products:

Intel® Optane™ Memory H20 with Solid State Storage

Intel® Optane™ Memory H10 with Solid State Storage

Intel® Optane™ Memory M10 Series

Intel® Optane™ Persistent Memory

Intel® Optane™ DC SSD Series

Intel® Optane™ SSD 9 Series

So the above Intel products are read by claim 17 of ‘653 patent under Doctrine of Equivalence.

COUNT I: INFRINGEMENT OF U.S. PATENT NO. 6744653

11. Plaintiff Mr. Huang refers to and incorporates herein the allegations of Paragraphs 1-10 above.

12. On June.1, 2004, U.S. Patent No.6,744,653 (the “‘653 Patent”) was duly and legally issued for a “CAM cells and differential sense circuit for content addressable memory (CAM).” A true and correct copy of the ‘653 patent is attached hereto as Exhibit B. Xiaohua Huang as inventor is the owner of all rights, title, and interest in and to the ‘653 patent.

13. On information and belief, Defendant have infringed and continue to infringe directly, indirectly on Doctrine of Equivalence one or more of the claims of the ‘653 patent through making and selling:

Intel® Optane™ Memory H20 with Solid State Storage,

Intel® Optane™ Memory H10 with Solid State Storage,

Intel® Optane™ Memory M10 Series,
Intel® Optane™ Persistent Memory,
Intel® Optane™ DC SSD Series and
Intel® Optane™ SSD 9 Series

which have infringed at least claim 17 of the '653patent as analyzed in paragraph 6-10 under 35 U.S.C. § 271(a), (b) and(c).

14. On information and belief, Defendant have induced its Customers to have infringed and continue to infringe directly, indirectly on Doctrine of Equivalence one or more of the claims of the '653patent by transferring data through the accused devices which have infringed at least claim 17 of the'653patent as analyzed in paragraph 6-10 under 35 U.S.C. § 271(a), (b) and (c).

15. On information and belief, Defendant have made contributory infringement directly, indirectly on Doctrine of Equivalence to one or more of the claims of '653patent by its customers adding its SSD device to Internet which have infringed at least claim 17 of the'653patent as analyzed in paragraph 6-10 under 35 U.S.C. § 271(a), (b) and(c). The using of SSD devices accused as well as reading and writing data in Server and Storage are completely not a staple article or commodity of commerce suitable for substantial non-infringing use.

16. Defendant's acts of infringement, inducing infringement and contributory infringement have caused damage to Xiaohua Huang, and Xiaohua Huang is entitled to recover from Defendant for the damages sustained by Xiaohua Huang as a result of Defendant's wrongful acts in an amount subject to proof at trial. Defendant's infringement of Xiaohua Huang exclusive rights under the '653patent patent will continue to damage Xiaohua Huang, causing

irreparable harm for which there is no adequate remedy at law, unless enjoined by this Court. Defendant's infringement entitle Xiaohua Huang to recover damages under 35 U.S.C. § 284 and to attorneys' fees and costs incurred in prosecuting this action under 35 U.S.C. § 285.

JURY DEMAND

17. Pursuant to Fed. R. Civ. P. 38(b), Plaintiff Xiaohua Huang requests a trial by jury on all issues.

PRAYER FOR RELIEF

WHEREFORE, Xiaohua Huang prays for the following relief:

- (a). A judgment in favor of Xiaohua Huang that Defendant has infringed and is infringing U.S. Patent No 6744653;
- (b). A judgment that the '653 patent are valid and enforceable;
- (c). An order preliminarily and permanently enjoining Defendant and its subsidiaries, parents, officers, directors, agents, servants, employees, affiliates, attorneys and all others in active concert or participation with any of the foregoing, from further acts of infringement of the '653 patent;
- (d). An accounting for damages resulting from Defendant's infringement of the '653 patent under 35 U.S.C. § 284;
- (e). An assessment of interest on damages;
- (f). A judgment awarding damages to Xiaohua Huang for its costs, disbursements, expert witness fees, and attorneys' fees and costs incurred in prosecuting this action, with interest pursuant to 35 U.S.C. § 285 and as otherwise provided by law;
- (g). Such other and further relief as this Court may deem just and equitable.

Dated: November 15, 2021

Respectfully Submitted,

A handwritten signature in black ink, appearing to be 'XH' or similar initials, written in a cursive style.

/s/ Xiaohua Huang

P.O. Box 1639, Los Gatos CA95031

Tel: 669 273 5650

Email: paul_huang1010@outlook.com

Exhibit B US patent No. 67446531

From: Xiaohua Huang
P.O. Box 1639, Los Gatos, CA95031
Tel: 669-273-5633
Email: xiaohua_huang@hotmail.com
paul-huang1010@outlook.com

RECEIVED

November 19, 2021

CLERK, U.S. DISTRICT COURT
WESTERN DISTRICT OF TEXAS

BY: lad
DEPUTY

To: Ms. Jennifer Galindo-Beaver
U.S. District Clerk's Office
800 Franklin Ave., Room 380
Waco, Texas 76701

Dear Ms. Galindo-Beaver,

The enclosed is:

1. Complaint to Intel and exhibit US patent 6744653,
2. AO440 Summon
3. JS44 civil cover sheet
4. APPLICATION TO PROCEED IN DISTRICT COURT WITHOUT
PREPAYING FEES OR COSTS to waive for filing fee.

Best Regards

xiaohua Huang

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FROM: X. Huang
P.O. BOX. 1639
LOS Gatos, CA 95031

TO:

Ms. Jennifer Galindo-Beaver
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800 Franklin Ave, Room 380
Waco, Texas 76701

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